Amendments to the Specification

Please amend paragraph **[0003]** as follows:

[0003] More recently developed devices such as the flash-EEPROM device have provided the ability to ~~used~~ use normal electrical voltages for erasure as well as providing for partial erasures. As such erasures and subsequent reprogramming are possible at essentially "normal" semiconductor speeds, flash-EEPROM devices are also generally referred to as a flash random access memory device or flash-RAM. With the increased performance of the flash-RAM, it has become desirable to increase the density of the memory storage units which generally encompass both a floating gate and a control gate for each unit. One problem with forming devices with such increased density has been the forming of the floating gate structures using generally known photolithographic methods. Therefore it would be desirable to provide alternative methods for forming floating gate transistor structures as well as the structures formed employing such methods.

Please amend paragraph **[0032]** as follows:

[0032] Referring now to Fig. 8, another embodiment 10b of the present invention is depicted where a conductive floating gate material layer 62b is formed having a reduced thickness from that of floating gate material layer 62 depicted in Fig. 5. As shown, floating gate material layer 62b is formed having a thickness which is less than the amount second portion 28 (Fig. 4) extends outwardly from surface 42 of semiconductive material 12. Thus, when floating gate material layer 62b is planarized, as shown in Fig 9, a floating gate material portion or floating gate 64b is formed that only partially fills recess 70 and which has an outermost surface 48 which is essentially concave in cross-section. Outermost surface 48 has a surface area which is greater than a surface that is essentially straight across in cross-sectional view. In addition, while not depicted, it will be understood that outermost surface 48 of floating gate 64b can be roughened analogous to that of outermost roughened surface 46 shown in Fig. 7. Thus by providing floating gate 64b having a roughened outermost surface, the surface area of such a surface can be further increased, if desired.

Am ndments to the Claims

Claims 1-69 (Canceled).